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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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R. BURNS ISRAELSEN
WORKMAN NYDEGGER
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, UT 84111

EXAMINER
WILLIAMS, HOWARD L

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/682,106	**Applicant(s)** DOUMA ET AL.	
	Examiner Howard L. Williams	**Art Unit** 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Claims 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what means for inducing is. The terminology is misdescriptive of an inductor. The examiner suggests means for providing an inductance.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9-17, 20 and 21 are rejected under 35 U.S.C. 102(b) as clearly anticipated by Telefus et al (US 2002/0008501).

Your claim:	Telefus
1. A boost converter for use in a transceiver to generate an output voltage that is greater than a voltage available to the boost converter, the boost converter comprising:	fig 3b.
an inductor adapted to couple at a first end of the inductor to a power supply',	8
a switch that is adapted to couple a second end of the inductor to the return of the power supply when the switch is closed;	Q1
a diode coupled at the anode to the second end of the inductor;	10
a capacitor coupled to a cathode of the diode and adapted to couple to the return path of the power supply, the capacitor adapted to maintain an output voltage;	12
microprocessor for monitoring the output voltage, wherein the microprocessor generates a pulse width modulated signal in response to the output voltage; and	210
a gate coupled to the pulse width modulated siral and to a pulse train, the gate producing a modulated pulse train, the gate further coupled to the switch such that the modulated pulse train can be used to control the switch and move the output voltage to a target voltage.	220

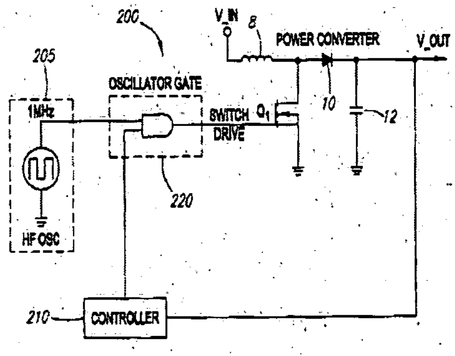

FIG. 3b

2. The boost converter set forth in claim 1, the pulse train being a signal between about 500 kHz and 10 MHz	The oscillator 220 is labeled in fig. 3B as operating at 1MHZ.
3. The boost converter set forth in claim 1, the pulse width modulated signal being a signal between about 10 kHz and 1 MHz.	Telefus discloses a framing generator for the PWM and suggests 50KHz as one possible rate. Paragraph 0045.
4.The boost converter set forth in claim 1, wherein the gate is at least one of an AND gate, a transistor switch, and a field effect transistor.	Fig. 3b shows an AND gate.
5. The boost converter set forth in claim 1, further comprising an analog to digital (A/D) converter coupled between the output voltage and the microprocessor to derive a signal usable as a feedback signal by the microprocessor.	In conjunction with Fig. 6A the controller is implemented as an ADC and microprocessor.
9. The boost converter of claim 1, wherein the switch is a field effect transistor.	The switch Q1 is shown as an FET.
10. A boost converter for use in a transceiver to generate an output voltage that is greater than a voltage available to the boost converter from a power supply, the boost converter comprising:	See fig. 3b or 6a. From Telefus Fig. 3b
means for inducing coupled to a power supply;	8
means for switching coupled to the means for inducing, the means for switching adapted to allow a current to flow from the power supply through the means for inducing;	Q1
means for storing coupled through a means for blocking to the means for inducing, the means for storing adapted to maintain an output voltage caused by current flowing through the means for blocking to the means for storing;	10, 12
means for controlling coupled to the means for storing, the means for storing being adapted to monitor the output voltage across the means for storing and for generating a control signal to control the means for switching; and	210
means for gating coupled to the means for controlling and the means for switching, the means for gating using the control signal to modulate a pulse train to control the means for switching.	220

11. The transceiver boost converter as set forth in claim 10, further comprising a means for digitizing coupled between the means for storing and the means for controlling, the means for digitizing adapted to derive a signal from the output voltage that is useable by the means for controlling.

12. A boost converter for use in a transceiver to generate an output voltage that is greater than a voltage of a power supply available to the boost converter, the boost converter comprising:

a capacitor used to generate an output voltage, wherein the capacitor is coupled to an inductor through a diode;

a switch that is coupled to the diode and the inductor such that current flows through the diode and the capacitor when the switch is off and such that current flows through the switch when the switch is on;

a microprocessor that monitors the output voltage and that generates a pulse width modulated signal in response to the output voltage; and

a gate generates a modulated pulse train by gating the pulse width modulated signal with a pulse train, wherein the modulated pulse train turns the switch on and off in a manner that raises the output voltage to a target voltage.

13. A boost converter as defined in claim 12, wherein the gate is one of an AND gate, a transistor switch, and a field effect transistor.

14. A boost converter as defined in claim 12, wherein the pulse width modulated signal being a signal between about 10 kHz and 1 MHz.

15. A boost converter as defined in claim 12, wherein the pulse train signal is between about 500 kHz and 10 MHz.

16. A boost converter as defined in claim 12, wherein the switch is a field effect transistor, wherein a gate of the field effect transistor is connected to the modulated pulse train.

17. A boost converter as defined in claim 12, further comprising an analog to digital (A/D) converter coupled between the output voltage and the microprocessor to derive a signal usable as a feedback signal by the microprocessor.

Telefus shows the ADC and microprocessor in fig. 6a.

Telefus fig. 6a

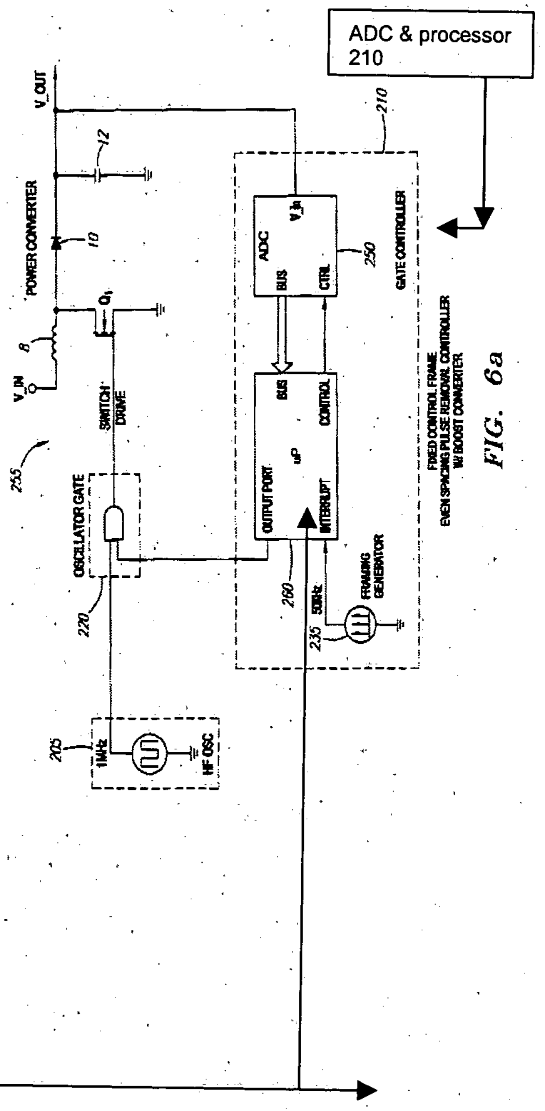

FIG. 6a

20. A method of generating a voltage in a transceiver for a diode used in the transceiver, the diode requiring a voltage greater than voltages available to the transceiver via an external power supply the method comprising:	See fig. 3b or 6a. From Telefus Fig. 6a
receiving a current from a power supply;	Vin
passing the current through an inductor;	8
passing the current from the inductor through a diode;	10
passing the current from the diode through a capacitor to create an output voltage;	12
feeding at least a portion of the output voltage into a microprocessor; at the microprocessor, generating a pulse width modulated signal in response to the output voltage;	210, 250, 260
generating the pulse width modulated signal with a pulse train to produce a modulated pulse train; and	205
controlling a switch with the modulated pulse train, the switch connected to the inductor such that the current passes through the inductor and the switch to ground when the switch is on and such that stored energy in the inductor causes the current to pass through the diode further through the capacitor when the switch is switched from on to off thereby controlling the output voltage.	Q1
21. The method of claim 20, wherein feeding at least a portion of the output voltage into a microprocessor further comprises: feeding the output voltage into an analog to digital converter; and feeding the output of the analog to digital converter into the microprocessor.	210, 250, 260

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7, 18, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Telefus et al (US 2002/0008501) in view of Killat 6,448,745. Telefus et al. does not show a voltage divider to scale the sensed voltage input to the ADC. Killat shows a voltage divider Z11 and Z12 (front page) to scale the input to the ADC in a boost converter using digital control. It would have been obvious to combine the voltage divider of Killat in the Telefus et al boost converter because the use of the ADC mandates that its input signal be kept within its rated input so that a useful digital value representative of the input signal can be obtained.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Telefus et al (US 2002/0008501) in view of Mitsuishi et al. (US 5736948 A). While Telefus appears to show in figure 6A the ADC and processor on the same chip, it is not entirely clear. Mitsuishi et al shows on the front page the ADC internal to the microprocessor. Col. 1 lines 10-24. It would have been obvious to utilize the single chip microcomputer disclosed in Mituishi et al. in Telefus for its compact incorporation of conversion and enchanced control.

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office has a new central facsimile number for application specific correspondence intended for entry, it is 703-872-9306.

Howard L. Williams

5/28/04
Voice 571.272.1815

Howard L. Williams
Primary Examiner
Art Unit 2819